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EXAMINER	
VAZQUEZ, ARLEEN M	
ART UNIT	PAPER NUMBER
2829	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/06/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/716,686	VERMEIRE ET AL.	
	Examiner	Art Unit	
	Arleen M. Vazquez	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-59* is/are pending in the application.

4a) Of the above claim(s) *5,27-30,33-39 and 48-59* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-18,31,32 and 40-47* is/are rejected.

7)☒ Claim(s) *19-26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election with traverse of Species of Figure 13 claims 1-26,31-32 and 40-44 in the reply filed on 12/26/2006 is acknowledged.

Claim 5 has been withdrawn from consideration because it does not read on species of Figure 13 elected by applicant.

The traversal is on the ground(s) that oversample prognostic cell shown in Figure 16, including claims 45-47, is a configuration of any one of the species of prognostic cells to include a plurality of test devices and provide multiple readout capability and thus is generic to all species. This is found persuasive and restriction on Species of Figure 16 and claims 45-47 has been **withdrawn.** Claims 45-47 are being rejoined to the prosecution considered as generic claims readable in any of the species of prognostic cells.

Claims 1-4,7-26,31-32 and 40-47 are going to be examined.

2. Claims 5,27-30,33-39 and 48-59 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected Species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 12/26/2006.

Claim Objections

3. Claims 31 and 32 are objected to because of the following informalities:

In claims 31, the limitation of "the host IC" should be changed to "the integrated circuit (IC) chip" to avoid lack of antecedent basis.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-26,31-32 and 40-47 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1,15,40 and 45 it is not clear what means "a prognostic distance". The distance if referring to a "physical distance from the useful circuit and the prognostic cell" or is referring to "a value determined by the two components". Clarification is requested.

Claim 2 states that a failure indicator will be generated if the stress test component fails but claim 2 depends from claim 1 and claim 1 states that a failure indicator will be generated because of the failure of the useful circuit. It is not clear then which device (circuit or component) is being tested in order to indicate the failure or how are this two device related in order to generate the failure indicator because the useful circuit is outside the prognostic cell and the stressed test component is part of the prognostic cell.

In claim 7 it is not clear what comprises "enhance measurement sensitivity". In what degree or by what parameters can be determined better measurement sensitivity between different devices.

Claims 40 and 45 indicate that the useful circuit will fail because of operational stress and further states that a failure indicator will be generated when the stress test

component. It is not clear then which device (circuit or component) is being tested in order to indicate the failure or how are this two device related in order to generate the failure indicator because the useful circuit is outside the prognostic cell and the stressed test component is part of the prognostic cell.

In claims 44 and 47,it is not clear what a "premature trigger" comprises and how are related "the number of test devices" with "the amount of useful lifetime sacrificed is less than an acceptable amount".

Claims 12 and 13 recites the limitation "the reference sub-circuit" in lines 1 and 2 of each claim. Is this refereeing to the "reference circuit" or the "reference circuit" has more circuits on its inside identify as sub-circuits? There is insufficient antecedent basis for this limitation in the claim.

Claim 41 recites the limitation "the host device" in line 4. Is "the host device" referring to "the useful circuit" or "the integrated circuit". There is insufficient antecedent basis for this limitation in the claim.

Claims 3-4,6,8-11,14,16-26,32,41-43 and 46 not specifically addressed share same indefiniteness from previous rejected claims.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4,6-14,16-18 and 40-43 and 45-46 are rejected under 35 U.S.C. 102(b) as being anticipated by ***Okandan et al. (US 6,348,806).***

As to claim 1, ***Okandan et al.*** discloses in Figures 1 and 2 an integrated circuit chip (10) comprising a useful circuit (26) having a component (transistor) that is subject to failure in response to operational stress (voltage stress supply by VDD), a prognostic cell (20,22,24) that is statistically designed to fail under increased operational stress (every component has to be designed to have a lifetime cycle, having an useful time and a fail time) and correlated to the operational stress (voltage stress supply by VDD) on the useful circuit (26) by a prognostic distance ahead of the useful circuit (26), said cell (20,22,24) triggering a failure indicator (indicator signal QBI) as a predictor of impending failure of the useful circuit (26).

As to claim 2, ***Okandan et al.*** discloses in Figures 1 and 2 the prognostic cell (20,22,24) comprising a test device (30 and 32) having a test component (transistor), a coupling circuit (24) that couples the operational stress (voltage stress supply by VDD) applied to the useful circuit (26) to the test device (30 and 32), a stress circuit (22) that increases the operational stress applied to the test device (30 and 32) to accelerate deterioration of the test component (Col. 2 ln 56 –Col. 3 ln 11), and a comparison circuit (36,38,40,42,44) that compares a performance characteristic of the stressed test component (30 and 32) to the baseline (predetermined value on reference circuit 46 to avoid failure), determines whether the stressed test component (30 and 32, is a reflection of component 26) has failed and generates the failure indicator (QBI).

As to claims 3 and 4, ***Okandan et al.*** discloses in Figures 1 and 2 the useful circuit and the test device are equivalent devices (are transistors) and are different devices with similar components (are two different types of transistors but have similar components).

As to claim 6, ***Okandan et al.*** discloses in Figures 1 and 2 the test component (30 and 32) has a different dimensions (30 and 32 are P channel transistors and component 26 is N channel transistor) than the useful circuit's component (transistor) to enhance measurement sensitivity.

As to claim 7, ***Okandan et al.*** discloses in Figures 1 and 2 the coupling circuit (24) couples the test device (30 and 32) to at least one of a supply voltage (VDD) applied to the useful circuit (26).

As to claim 8, ***Okandan et al.*** discloses in Figures 1 and 2 the stress circuit (22) prolong the stress event (supply of electrical stress) to increase the operational stress (supply of voltage VDD) applied to test device (30 and 32).

As to claims 9 and 10, ***Okandan et al.*** discloses in Figures 1 and 2 the prognostic cell (20,22,24) comprises a plurality of test devices (30,32,34), said comparison circuit (36,38,40,42,44) triggering the failure indicator (QBI) when a certain fraction of the plurality (30,32,34) fail.

As to claims 11,12 and 13, ***Okandan et al.*** discloses in Figures 1 and 2 a reference circuit (46) that is subjected to reduce operation stress to establish the baseline for the performance characteristic (Col. 4 Ins 20-34).

As to claim 14, ***Okandan et al.*** discloses in Figures 1 and 2 the increased operational stress (supply by 22 and VDD) accelerates an end-of-life failure mechanism (Col. 3 lns 3-12) of the prognostic cell (20,22,24).

As to claim 16, ***Okandan et al.*** discloses in Figures 1 and 2 the increased operational stress (supply by 22 and VDD) applied to the prognostic cell (20,22,24) is the same operational stress that is applied to the useful circuit (26) just increased so that the failure of the prognostic cell, although accelerated, tracks the failure of the useful circuit (26).

As to claim 17, ***Okandan et al.*** discloses in Figures 1 and 2 the operational stress (supply by 22 and VDD) comprises use stress and environmental stress (operational voltage VDD have use and environmental stress because includes variables such as operating voltage and operating current).

As to claim 18, ***Okandan et al.*** discloses in Figures 1 and 2 the operational stress (supply by 22 and VDD) is increased by an elevated supply voltage (the more time the operational voltage VDD is supply to the test device make unit of time to increase the voltage supply).

As to claims 40 and 45, ***Okandan et al.*** discloses in Figures 1 and 2 an integrated circuit chip (10) comprising a useful circuit (26) having a component (transistor) that is subject to failure in response to operational stress (voltage stress supply by VDD), an oversampled prognostic cell (20,22,24) with multiple readout capability (as shown in Figures 4 and 5) that is statistically designed to fail under increased operational stress (every component has to be designed to have a lifetime

cycle, having an useful time and a fail time) by a prognostic distance ahead of the useful circuit (26) component, said prognostic cell (20,22,24) comprising a plurality of test devices (30,32,34) each having a test component (transistor or capacitor), a coupling circuit (24) that couples the operational stress (voltage stress supply by VDD) applied to the useful circuit (26) to the test devices (30,32,34), a stress circuit (22) that increases the operational stress applied to the test devices (30,32,34) as a function o the prognostic distance to accelerate deterioration of the test component (Col. 2 ln 56 –Col. 3 ln 11), and a comparison circuit (36,38,40,42,44) that compares a performance characteristic of the stressed test component (30 and 32) to the baseline (predetermine value on reference circuit 46 to avoid failure), determines whether the stressed test component (30 and 32, is a reflection of component 26) has failed and generates the failure indicator (QBI).

As to claim 41, ***Okandan et al.*** discloses in Figures 1 and 2 the coupling circuit (24) couples the test device (30 and 32) to at least one of a supply voltage (VDD) applied to the host device (10) and the stress circuit (22) prolong the stress event (supply of electrical stress) to increase the operational stress (supply of voltage VDD) applied to test device (30 and 32).

As to claim 42, ***Okandan et al.*** discloses in Figures 1 and 2 said comparison circuit (36,38,40,42,44) reads out each test device failure (each signal QBI correspond to one test device at the time).

As to claims 43 and 46, ***Okandan et al.*** discloses in Figures 1 and 2 a reference circuit (46) that is subjected to reduce operation stress to establish the baseline for the performance characteristic (Col. 4 lns 20-34).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over ***Okandan et al. (US 6,348,806)*** in view of ***Thomson et al. (US 5,117,113).***

As to claim 31, ***Okandan et al.*** discloses everything above except for the prognostic cell predicts threshold voltage shift of a MOS device in the host IC based on radiation effects, said prognostic cell comprising test and reference MOS devices with different gate bias conditions so that the MOS devices exhibit different threshold voltage shifts when subjected to ionizing radiation, and a comparator circuit that generates the failure indicator when the difference in threshold voltages exceeds a preset amount. However, ***Thomson et al.*** discloses in Figure 2 a prognostic cell predicts threshold voltage shift of a MOS device (1 or 2) in the host IC (chip where the devices a located) based on radiation effects, said prognostic cell comprising test (1) and reference (2) MOS devices with different gate bias conditions (their gates are connected to different sources, device 1 have gate connected to VDD and device 2 have gate connected to ground) so that the MOS devices (1 and 2) exhibit different

threshold voltage shifts when subjected to ionizing radiation (see abstract), and a comparator circuit (7) that generates the failure indicator when the difference in threshold voltages exceeds a preset amount (Col.6 lns 20-22).

It would have been obvious for one ordinary skill in the art at the time the invention was made to modify ***Okandan et al.*** teachings by having a prognostic cell predicts threshold voltage shift of a MOS device in the host IC based on radiation effects as thought as ***Thomson et al.*** for detecting and quantifying ionizing radiation through the transistors of the devices to be tested and in this way determining the reliability of the devices.

As to claim 32, ***Okandan et al.*** discloses everything above except for a worst case gate bias is applied to the test MOS device and a best case gate bias is applied to the reference MOS device. However, ***Thomson et al.*** discloses in Figure 2 a worst case gate bias (maximum voltage VDD applied to gate of device 1) is applied to the test MOS device (1) and a best case gate bias (minimum voltage Ground applied to gate of device 2) is applied to the reference MOS device (2).

It would have been obvious for one ordinary skill in the art at the time the invention was made to modify ***Okandan et al.*** teachings by having a worst and a best gate bias applied to two different MOS devices as thought as ***Thomson et al.*** in order to determined the difference between the devices so the failure can be determined.

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sasaki et al. (US 4,833,395) discloses a "Semiconductor device having a test circuit".

Davies et al. (US 7,005,871) discloses an "Apparatus, system and method for managing aging of an integrated circuit".

Arabi et al. (US 6,005,407) discloses an "Oscillation-based test method for testing an at least partially analog circuit".

Manna et al. (US 6,724,214) discloses a "Test Structures for on-chip real-time reliability testing".

Allowable Subject Matter

10. Claims 19-26 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In claim 19, the prior art of record taken alone or in combination fail to teach or disclose the useful circuit's component has a cumulative failure probability C(t) and the prognostic cell has a cumulative trigger probability P(t), t1 equals the time at which a fraction f1 of the prognostic cells have triggered, t2 equals the time at which the failure probability of the useful circuit's component has increased to a fraction f2, said prognostic distance being equal to t2-t1.

Claims 20-26 depends from dependent claim 19 and would also be allow.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arleen M. Vazquez whose telephone number is 571-272-2619. The examiner can normally be reached on Monday to Friday, 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ha Nguyen can be reached on 571-272-1678. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AMV

HA TRAN NGUYEN
SUPERVISORY PATENT EXAMINER

3/3/7